Specification Amendments

Please replace paragraph 0018 with the following rewritten paragraph:

0018 Fig. 3 first shows the results of stripping the first patterned photoresist layer 16, the series of patterned silicon nitride layers 14 and the series of patterned pad dielectric layers 12 from the semiconductor substrate 10. The foregoing layers may be stripped employing methods and materials as are conventional in the semiconductor product fabrication art. Typically, the first patterned photoresist layer will be stripped employing an appropriate photoresist stripping material (either dry plasma, wet chemical or mixture thereof). The series of patterned silicon nitride layers is typically stripped employing a phosphoric acid stripping solution. The series of patterned pad dielectric layers is typically stripped employing an aqueous hydrofluoric acid containing etchant.

Please replace paragraph 0023 with the following rewritten paragraph:

0023 Fig. 5 shows the results of ion implanting exposed

corner region portions of the active region of the semiconductor substrate 10 within the memory region RM to form a series of corner implanted regions 22. The ion implanting is undertaken employing a dopant polarity as is appropriate for the semiconductor substrate 10. Typically, the corner implanted regions are have a dopant concentration of from about 1E18 to about 1E20 dopant atoms per cubic centimeter. They also serve as capacitor node layers within a series of storage capacitors formed incident to further processing of the semiconductor product of Fig. 5.

Please replace paragraph 0027 with the following rewritten paragraph:

0027 Fig. 7 first shows the results of forming a series of gate electrodes 26 upon the series of gate and capacitor dielectric layers 24 within the logic region RL and memory region RM of the semiconductor substrate. Fig. 7 also shows a series of capacitor plate layers 26' formed upon the series of gate and capacitor dielectric layers 24 within the memory cell region RM and mirroring the series of corner implanted regions 22 such as to form a series of storage capacitors. Fig. 7 finally shows an interconnect layer 26'' formed upon the etched elongate[[s]]d

isolation region 18'' within the memory region RM of the semiconductor substrate 10.